PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H01L 21/00 — A1

(11) International Publication Number: WO 99/41773

(43) International Publication Date: 19 August 1999 (19.08.99)

(21) International Application Number: PCT/US99/02742

(22) International Filing Date: 8 February 1999 (08.02.99)

(30) Priority Data:
09/022,134 11 February 1998 (11.02.98) US

(71) Applicant: APPLIED MATERIALS, INC. [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventor: JENNINGS, Dean, C.; 2898 Morgan Drive, San Ramon, CA 94583 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

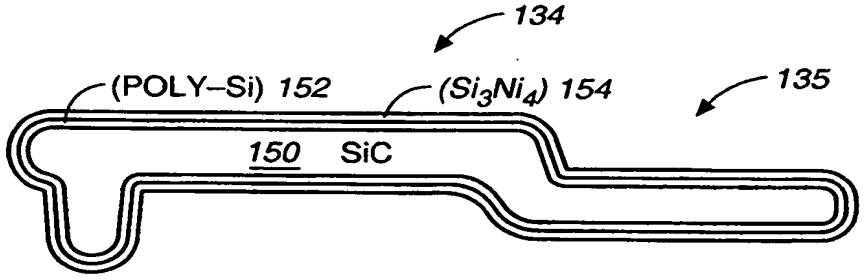
(81) Designated States: JP, KR, European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: SUBSTRATE SUPPORT FOR A THERMAL PROCESSING CHAMBER

(57) Abstract

A semiconductor wafer support for use in a thermal processing chamber includes a shelf for receiving a semiconductor wafer. The wafer support is formed of a silicon carbide substrate having a polysilicon layer disposed on the substrate, and a silicon nitride layer disposed on the polysilicon layer. A method of forming the multi-layered semiconductor wafer support is also disclosed.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania
AM	Armenia
AT	Austria
AU	Australia
AZ	Azerbaijan
BA	Bosnia and Herzegovina
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CU	Cuba
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GH	Ghana
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IL	Israel
IS	Iceland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgyzstan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakstan
LC	Saint Lucia
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LS	Lesotho
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
MK	The former Yugoslav Republic of Macedonia
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TM	Turkmenistan
TR	Turkey
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam
YU	Yugoslavia
ZW	Zimbabwe

SUBSTRATE SUPPORT FOR A THERMAL PROCESSING CHAMBER

Background

This invention relates to a substrate support for a thermal processing chamber.

In many semiconductor device manufacturing processes, the required high levels of device performance, yield, and process repeatability can only be achieved if the temperature of the substrate (e.g., a semiconductor wafer) is tightly monitored and controlled during processing of the substrate.

Rapid thermal processing (RTP), for example, is used for several different fabrication processes, including rapid thermal annealing (RTA), rapid thermal cleaning (RTC), rapid thermal chemical vapor deposition (RTCVD), rapid thermal oxidation (RTO), and rapid thermal nitridation (RTN). The temperature in an RTP chamber, however, may exceed 1100 °C and is subject to rapid change, thereby making precise control of the substrate temperature more complicated and more difficult.

Additionally, although it is desirable to provide a substantially uniform temperature throughout the substrate during many manufacturing processes, the support on which the substrate rests can affect the manufacturing system's ability to achieve such uniformity. In susceptorless systems, for example, the substrate is usually only supported around its perimeter with an edge ring. In some situations, however, the edge ring acts as a thermal load which removes heat from the edge of the substrate, thereby making it difficult to provide a uniform temperature across the substrate and interfering with temperature measurements.

Summary

In general, in one aspect of the invention, a semiconductor wafer support includes a shelf for receiving a semiconductor wafer. The support is formed of a silicon carbide substrate, a polysilicon layer disposed on the silicon carbide substrate, and a silicon nitride layer disposed on the polysilicon layer. In one implementation, the wafer support is an edge ring that includes an annular support for receiving a semiconductor wafer.

In another aspect, a method of forming a semiconductor wafer support includes forming a silicon carbide substrate, providing a polysilicon layer on the substrate, and providing a silicon nitride layer on the polysilicon layer. The substrate can be annular-shaped.

Various implementations include one or more of the following features. The edge ring or other wafer support can be disposed in a thermal semiconductor processing chamber. The polysilicon layer, which can include intrinsic or doped polysilicon, can be disposed directly on the silicon carbide substrate. Similarly, the silicon nitride layer can be disposed directly on the polysilicon layer. The polysilicon and silicon nitride layers can cover substantially the entire surface of the silicon carbide substrate.

In one implementation, the silicon nitride layer has a thickness in the range of 1800-2000 angstroms, and the polysilicon layer has a thickness of approximately 100 microns. Other thicknesses, however, can be used for either or both of the layers. Thus, the silicon nitride layer can have thicknesses of less than or more than 2000 angstroms. The silicon nitride layer can form an anti-reflective coating.

Although the wafer support or edge ring can be made using many different techniques, according to one technique, the polysilicon layer is grown in an epitaxial reactor, and the silicon nitride layer is grown using a low pressure chemical vapor deposition process.

Various implementations include one or more of the following advantages. The addition of the silicon nitride layer can improve the emissivity of the edge ring or other substrate support. In some systems, an RTP temperature controller measures the chamber temperature and determines the power required to affect a temperature change. The higher emissivity of the edge ring allows it to absorb or emit the radiation from a heating element more quickly. The edge ring can, therefore, respond more quickly to temperature changes.

The silicon nitride layer also can prevent formation of an oxide layer during processing, thereby resulting in a more uniform temperature across the semiconductor substrate and more accurate temperature measurements. In addition, the silicon nitride layer can help reduce the occurrence of failures to a heating element in the chamber. Furthermore, the silicon nitride layer can act as a diffusion barrier to prevent impurities that may be present in the poly-Si layer from contaminating a semiconductor substrate supported by the edge ring.

Use of the silicon nitride layer allows the edge ring to behave like an extension of the substrate so that the temperatures and temperature changes of the edge ring and substrate coincide more closely with one another. As a result, the energy entering the chamber in which the edge ring is disposed can be more balanced throughout different parts of the chamber, and groups of lamps in the heating

element can be more easily controlled by the RTP temperature controller.

Additional features and advantages will be readily apparent from the following detailed description, drawings and claims.

Brief Description of the Drawings

FIG. 1 is an elevated partial cross-sectional view of an RTP system according to the present invention.

FIG. 2 is a cross-sectional side view of the RTP system according to the present invention.

FIG. 3 is a plan view of an edge ring according to the present invention.

FIG. 4 is a cross-sectional side view of the edge ring of FIG. 3 along line 3-3.

FIG. 5 is a cross-sectional side view of the edge ring of FIG. 3 illustrating further details according to one implementation of the present invention.

FIG. 6 is a flow chart for making an edge ring according to one implementation of the present invention.

Detailed Description

FIGS. 1 and 2 illustrate a rapid thermal processing (RTP) system including a processing chamber 100 for processing a disk-shaped silicon substrate 106. Various features of the RTP system are described in further detail in co-pending U.S. Patent Application Serial No. 08/641,477, entitled "Method and Apparatus for Measuring Substrate Temperatures", filed on May 1, 1996, which is incorporated herein by reference.

The substrate 106 is mounted inside the chamber on a substrate support structure 108 and is heated by a heating element 110 located directly above the substrate. The

heating element 110, which can include tungsten (W) halogen lamps 111, generates radiation 112 which enters the processing chamber 100 through a water-cooled quartz window assembly 114 disposed above the substrate. The lamps 111 can be arranged in multiple zones which are grouped together in several control groups. A temperature control algorithm is used to control the lamps and, thereby to control the temperature. Beneath substrate 106 is a reflector 102 which is mounted on a water-cooled, stainless steel base 116. The reflector 102 can be made of aluminum and has a highly reflective surface coating. The underside of substrate 106 and the top of reflector 102 form a reflecting cavity 118 for enhancing the effective emissivity of the substrate, thereby improving the accuracy of temperature measurement.

The temperatures at localized regions 109 of the substrate 106 are measured by a plurality of temperature probes 126 and pyrometers 128. The temperature probes 126, which can include fiber-optic probes, are distributed at varying distances from the center of the substrate 106.

During thermal processing, the support structure 108 is rotated. In one implementation, for example, the support structure is rotated at about 90 revolutions per minute. Thus, each probe samples the temperature profile of a corresponding annular ring area on the substrate. The support structure which rotates the substrate includes an edge ring 134 which contacts the substrate around the substrate's outer perimeter, thereby leaving all of the underside of the substrate exposed except for a small annular region about the outer perimeter.

The edge ring 134 rests on a rotatable tubular quartz cylinder 136 that is coated with silicon to render it opaque in the frequency range of pyrometers 128. The silicon coating on the quartz cylinder acts as a baffle to

block out radiation from external sources that might disturb the temperature measurements. The bottom of the quartz cylinder is held by an annular upper bearing race 142 which rests on a plurality of ball bearings 138 that are, in turn, held within a stationary, annular, lower bearing race 140.

Referring to FIGS. 3 and 4, edge ring 134 includes an annular shelf or lip 135 upon which the edge of substrate 106 rests. For an 8-inch (200 mm) semiconductor wafer, the edge ring 134 can have a outer diameter (d) of approximately 9.3 inches, and an inner diameter (D) of approximately 7.6 inches (190 mm). The annular shelf or lip 135 can have a radial width (w) of approximately 0.2 inches (5 mm). The edge ring 134 can also include an annular rib 137. The rib 137 provides structural support for the edge ring 134. The foregoing dimensions are suitable for use of the edge ring 134 in certain processing chambers, such as the RTP Centura™ or the RTP Centura XE ™, manufactured by Applied Materials, Inc. Other dimensions may be suitable for wafers of different sizes, for example, a 12-inch (300 mm) semiconductor wafer, or different processing systems.

Referring to FIG. 5, the main body of the edge ring 134 is formed from a silicon carbide (SiC) substrate 150. However, SiC is transparent to radiation in the frequency range used for temperature measurements of the substrate, and as a result, can transmit stray radiation that may affect the accuracy of the temperature measurement. Therefore, the edge ring 134 is coated with a layer of polysilicon (poly-Si) 152 to render it opaque to such radiation. In one implementation, a layer of intrinsic or doped poly-Si having a thickness of approximately 100 microns (μm) is formed directly over the entire top, bottom and side surfaces of the SiC substrate 150.

Providing a doped poly-Si layer on the SiC substrate can improve the low temperature absorption or emissivity of the edge ring 134 in the infrared range. That feature is advantageous because the temperature probes 126 and pyrometers 128 begin to detect temperatures of approximately 325 °C as the temperature of the wafer in the chamber 100 is raised. In some implementations, lower temperatures, for example, temperatures in the range of approximately 200-300 °C, are detected. By increasing the emissivity of the edge ring 134 in the infrared range, the edge ring 134 can be heated more quickly so that the edge ring does not act as a thermal load taking away heat at the edges of the semiconductor wafer 106.

The edge ring 134 further includes a layer of silicon nitride (Si_3Ni_4) 154 disposed directly on the poly-Si layer 152. In one implementation, a Si_3Ni_4 layer 154 of approximately 1800-2000 angstroms (Å) is formed over the entire surface of the poly-Si layer 152. In another implementation, a Si_3Ni_4 layer 154 as thin as approximately 1200 angstroms (Å) is formed over the poly-Si layer 152. Si_3Ni_4 layers having thicknesses less than 1200 angstroms or greater than 2000 angstroms also can be used.

In general, the Si_3Ni_4 layer 154 can improve the emissivity of the edge ring 134. The higher emissivity of the edge ring 134 makes it more responsive to the RTP temperature controller.

It has been observed, for example, that when an edge ring formed of SiC with an outer layer of poly-Si is heated during the manufacturing of a semiconductor substrate, an oxide layer can form on the poly-Si layer. The oxide layer typically grows at a different rate at the inner periphery of the edge ring 134 than at the outer periphery. The build-up of the oxide layer causes the portions of the edge

ring 134 near the inner periphery to heat up more quickly than portions of the edge ring near the outer periphery. Moreover, formation of an oxide layer on the underside of the edge ring 134, particularly in the vicinity of the annular shelf or lip 135, can effect measurements obtained through the temperature probes 126 as radiation is emitted or reflected from the underside of the edge ring 134.

The addition of the Si_3Ni_4 layer 154 can slow down or prevent formation of the oxide layer, thereby resulting in a more uniform temperature across the semiconductor substrate and more accurate temperature measurements.

In addition, use of the Si_3Ni_4 layer 154 can reduce the power consumption of some of the lamp zones in the heating element 110. Even if the total weighted energy is higher when the edge ring 134 is used, the power consumption of the zones of the heating element 110 can be controlled so that the energy entering the chamber 100 is more balanced. Also, in some implementations, the lamps 111 can use a lower average power than previously required because the edge ring 134 absorbs radiation from the lamps more efficiently. As such, the Si_3Ni_4 layer also can help reduce the occurrence of lamp failures.

The Si_3Ni_4 layer 154 also can act as a diffusion barrier to prevent metal impurities that may be present in the poly-Si layer 152 from contaminating the substrate 106.

As described above, the poly-Si and Si_3Ni_4 layers 152, 154 can be formed to cover substantially the entire surface of the edge ring 134. In other implementations, however, the poly-Si and Si_3Ni_4 layers 152, 154 need not cover the entire surface of the edge ring 134. Thus, the poly-Si and Si_3Ni_4 layers 152, 154 can be formed on the top surface only or the bottom surface only by using appropriate masks. For example, if the chamber 100 does not include the

reflector 102 to reflect radiation back to the bottom surface of the edge ring, the layers 152, 154 can be formed on the top surface of the edge ring only.

FIG. 6 illustrates one implementation for manufacturing the edge ring 134. As indicated by step 200, a block of SiC is formed, for example, using a chemical vapor deposition (CVD) process. Next, as indicated by step 202, the block of SiC is machined to form an annular ring having the desired dimensions of the edge ring 134. A diamond grinding head, for example, can be used to machine the SiC block to the desired dimensions. A poly-Si layer is grown on the surface of the machined SiC, as indicated by step 204. In one implementation, the poly-Si coating is grown in an epitaxial reactor at a temperature of approximately 1150-1200 °C at atmospheric pressure. Alternatively, the poly-Si layer can be formed by a deposition process using two masks, one for each of the top and bottom surfaces of the edge ring 134. After formation of the poly-Si layer, an Si_3Ni_4 layer is formed, as indicated by step 206. In one implementation, a low pressure CVD process is used to grow the Si_3Ni_4 layer. In general, the edge ring 134 should be kept free of contamination and contact with metal as well as bare hands and other media which may transfer oils, metals or salts. As indicated by step 208, a cleaning process can be performed immediately following manufacture of the edge ring as well as just prior to insertion of the edge ring in the chamber 100.

Although the specific semiconductor substrate support described above is an edge ring 134, a SiC substrate with a layer of poly-Si disposed on the SiC and a layer of Si_3Ni_4 disposed directly on the poly-Si layer can be used as the semiconductor wafer support in a susceptor system as

well. In such systems, the semiconductor wafer is placed on the susceptor support so that the amount of support is proportional to the surface area of the wafer.

Additionally, in many implementations, the edge ring 134 can have different dimensions from the specific dimensions described above. Similarly, the precise shape of the edge ring 134 may differ from that shown in FIGS. 3-5. For example, the annular shelf or lip 135 can have a sloped or beveled surface.

Other implementations are within the scope of the following claims.

What is claimed is:

1. A semiconductor wafer support comprising:

a shelf for receiving a semiconductor wafer, the support being formed of a silicon carbide substrate, a polysilicon layer disposed on the silicon carbide substrate, and a silicon nitride layer disposed on the polysilicon layer.

2. The semiconductor wafer support of claim 1 wherein the support is disposed in a thermal processing chamber.

3. The semiconductor wafer support of claim 1 wherein the support is disposed in a semiconductor processing chamber.

4. The semiconductor wafer support of claim 1 wherein the polysilicon layer is disposed directly on the silicon carbide substrate.

5. The semiconductor wafer support of claim 1 wherein the silicon nitride layer is disposed directly on the polysilicon layer.

6. An edge ring comprising:

an annular support for receiving a semiconductor wafer, the edge ring being formed of a silicon carbide substrate having a polysilicon layer disposed on the substrate, and a silicon nitride layer disposed on the polysilicon layer.

7. The edge ring of claim 6 wherein the edge ring is disposed in a thermal processing chamber.

8. The edge ring of claim 6 wherein the edge ring is disposed in a semiconductor processing chamber.

9. The edge ring of claim 6 wherein the polysilicon layer is disposed directly on the silicon carbide substrate.

10. The edge ring of claim 6 wherein the polysilicon layer comprises doped polysilicon.

11. The edge ring of claim 6 wherein the silicon nitride layer is disposed directly on the polysilicon layer.

12. The edge ring of claim 6 wherein the silicon nitride layer is disposed directly on the polysilicon layer.

13. The edge ring of claim 6 wherein the polysilicon and silicon nitride layers cover substantially the entire surface of the silicon carbide substrate.

14. The edge ring of claim 6 wherein the silicon nitride layer has a thickness of less than 2000 angstroms.

15. The edge ring of claim 6 wherein the silicon nitride layer has a thickness in the range of 1800-2000 angstroms.

16. The edge ring of claim 6 wherein the polysilicon layer has a thickness of approximately 100 microns.

17. The edge ring of claim 6 dimensioned to support a semiconductor wafer.

18. The edge ring of claim 6 wherein the polysilicon and silicon nitride layers form an anti-reflective coating.

19. A method of forming a semiconductor wafer support, the method comprising:

forming a silicon carbide substrate;

providing a polysilicon layer on the substrate; and

providing a silicon nitride layer on the polysilicon layer.

20. The method of claim 19 wherein forming a silicon nitride substrate comprises forming an annular-shaped substrate.

21. The method of claim 19 wherein providing a polysilicon layer comprises growing a polysilicon layer in an epitaxial reactor.

22. The method of claim 19 wherein providing a polysilicon layer comprises growing a polysilicon layer having a thickness of approximately 100 microns.

23. The method of claim 19 wherein providing a silicon nitride layer comprises growing a silicon nitride layer using a chemical vapor deposition process.

24. The method of claim 19 wherein providing a silicon nitride layer comprises growing a silicon nitride

layer using a low pressure chemical vapor deposition process.

25. The method of claim 19 wherein providing a silicon nitride layer comprises growing a silicon nitride layer having a thickness in the range of approximately 1800-2000 angstroms.

26. The method of claim 19 wherein providing a silicon nitride layer comprises growing a silicon nitride layer directly on the polysilicon layer.

27. The method of claim 19 wherein providing a polysilicon layer comprises depositing a doped polysilicon layer on the silicon carbide substrate.

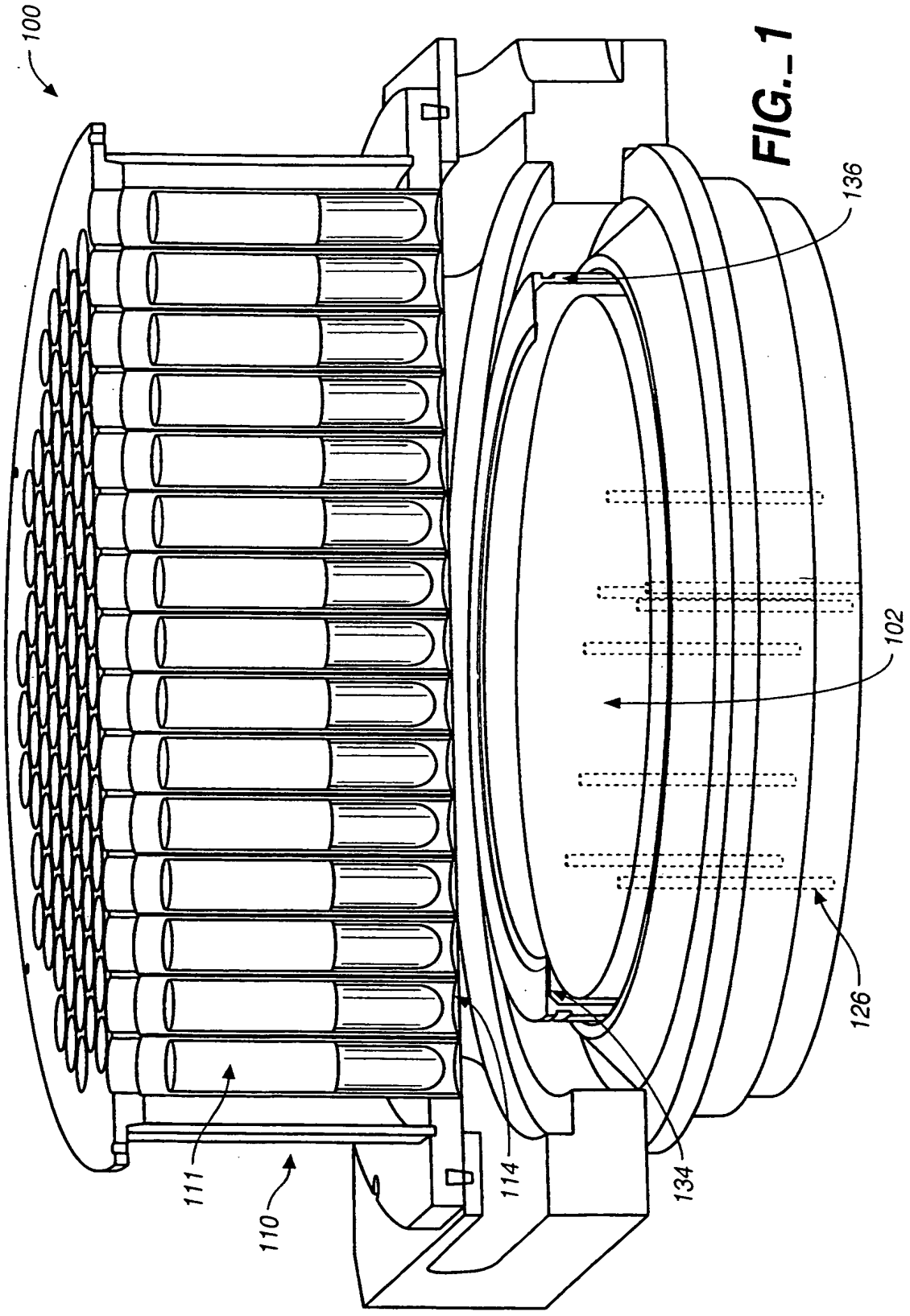


FIG._1

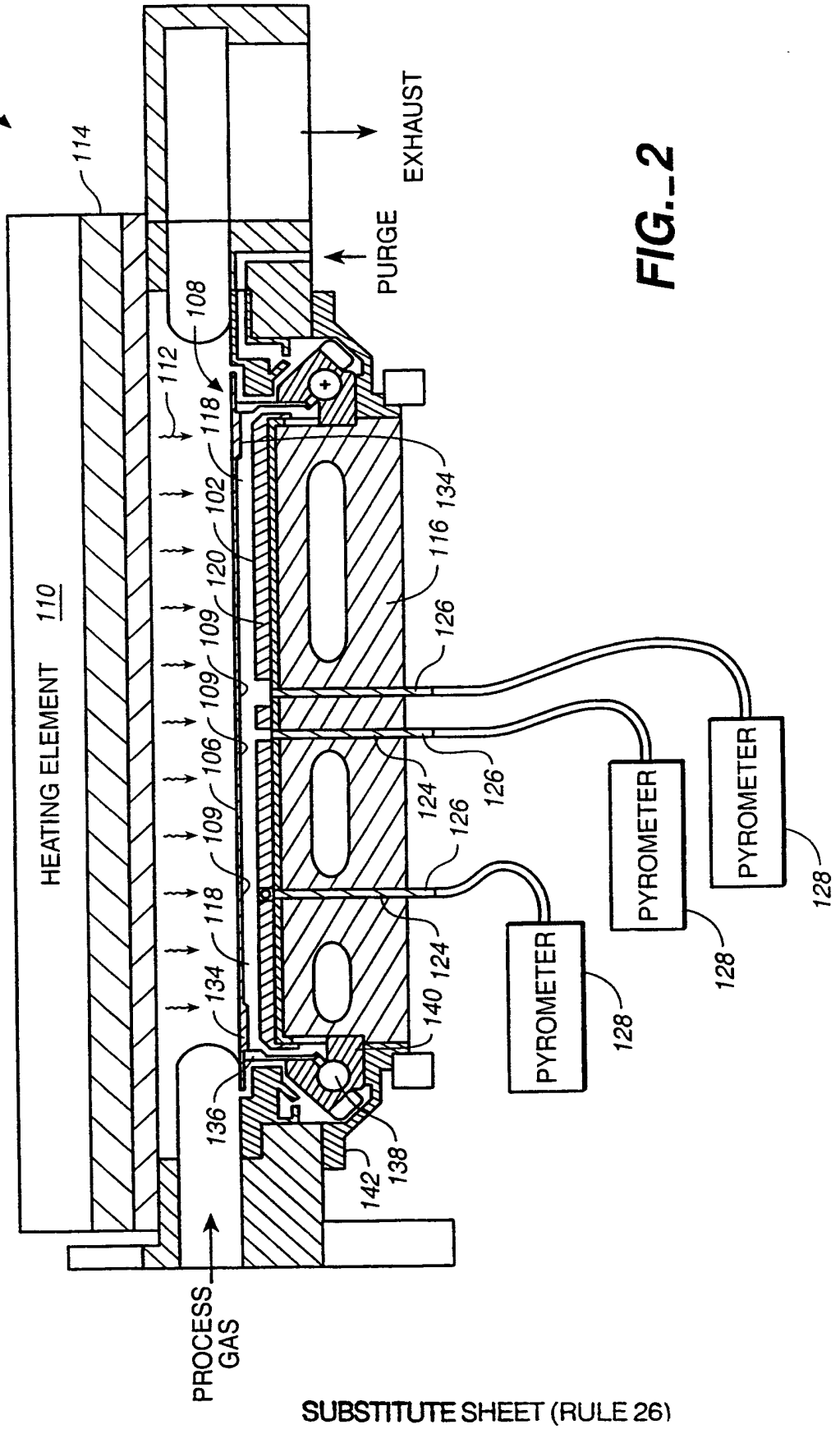


FIG._2

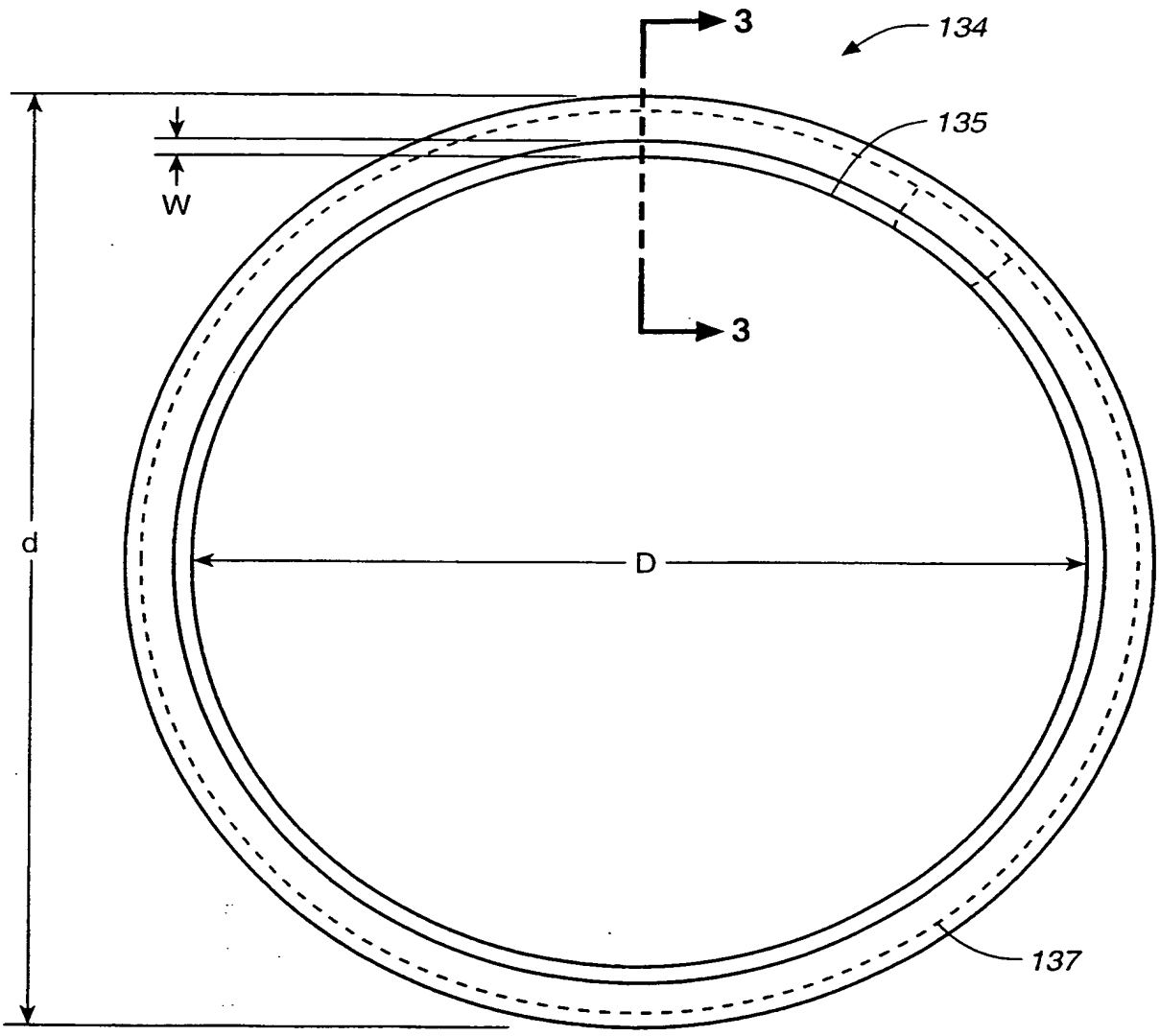


FIG._3

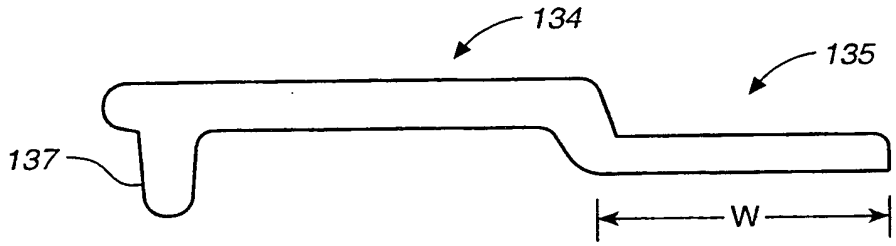


FIG._4

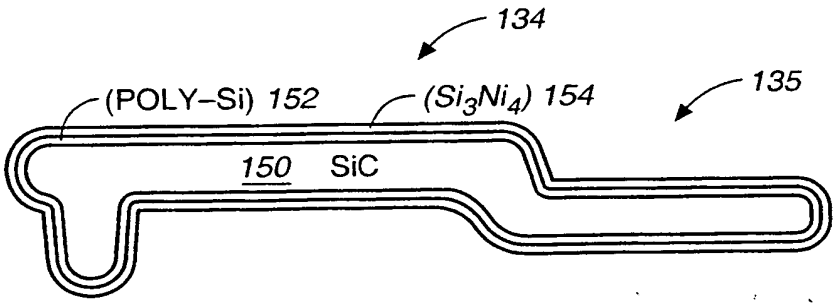


FIG._5

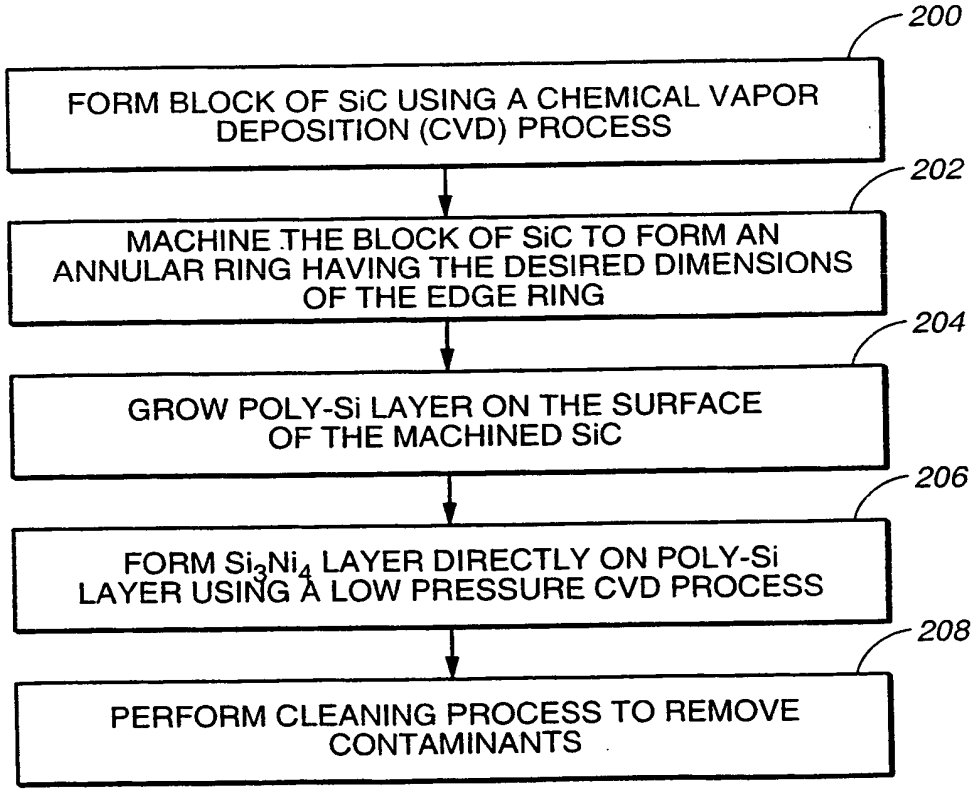


FIG._6

INTERNATIONAL SEARCH REPORT

Inte onal Application No
PCT/US 99/02742

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L21/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 5 458 688 A (WATANABE) 17 October 1995 see column 6, line 3-6	1-3,6-8, 17,19,20
A	EP 0 713 245 A (SHIN-ETSU HANDOTAI COMPANY) 22 May 1996 see abstract	1-3,6-8, 19,23-25
P,X	EP 0 840 358 A (APPLIED MATERIALS, INC.) 6 May 1998 see column 5, line 48 - column 6, line 33	1-9, 11-13, 16-20, 22,26

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 June 1999	09/06/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Oberle, T

1

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

Intr ional Application No
PCT/US 99/02742

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5458688 A	17-10-1995	JP 6260438 A	16-09-1994
		JP 6275599 A	30-09-1994
		JP 7122513 A	12-05-1995
		US 5482558 A	09-01-1996
		US 5482559 A	09-01-1996
EP 0713245 A	22-05-1996	JP 8148552 A	07-06-1996
		US 5759426 A	02-06-1998
EP 0840358 A	06-05-1998	JP 10173032 A	26-06-1998